Amendments to the Drawings:

The attached sheet of drawings including Figs. 1A-1B and 2-3 replaces the original sheet of drawings including Figs. 1A-1B and 2-3.

Fig. 3: Add a "PRIOR ART" label.

Attachment: Replacement Sheet containing Figs. 1A-1B and 2-3.

REMARKS

Claims 8-10 and 15-25 are pending in this application. Claims 1-7, 11-14, and 26-53 were previously canceled. Fig. 3 has been designated as "PRIOR ART." Accordingly, no new matter has been added.

Drawings

The Examiner has noted that Fig. 3 should be designated as "PRIOR ART.

The attached sheet of drawings including Figs. 1A-1B and 2-3 replace the original sheet of drawings including Figs. 1A-1B and 2-3. Fig. 3 has been revised to properly indicate the designation "PRIOR ART," as suggested by the Examiner. Accordingly, it is respectfully submitted that the drawings are in full compliance with 37 C.F.R. § 1.84.

Claim Rejections Under 35 U.S.C. § 102

Claims 8-10 and 15-25 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Applicant's Prior Art (Fig. 2), hereinafter "APA."

Withdrawal of the rejection of claims 8-10 and 15-25 is respectfully requested for at least the following reasons.

Patentability of Claims 8-10 and 15-25 over the APA

Claim 8 recites, inter alia:

> at least one substrate-biased silicon diode responsive to the signals from the signal pad for providing electrostatic discharge protection.
>
> [underline emphasis added]

Claim 23 recites, inter alia:

> a first plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals...
>
> a second plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals....
>
> [underline emphasis added]

The APA does not disclose or suggest an integrated circuit device having substrate-biased silicon diode(s) responsive to the signals from the signal pad for providing electrostatic discharge protection.

The APA shown in Fig. 2 is a known ESD protection scheme using dual diodes. The APA combination of the dual-diode structures and V_{DD}-to-V_{SS} ESD clamp circuit provides a path for an ESD current 2 to discharge, instead of through the internal circuits. When ESD current 2 is provided to signal a pad PAD1, and with a signal pad PAD2 relatively grounded, ESD current 2 is conducted to V_{DD} through Dp1. ESD current 2 is discharged to V_{SS} through the V_{DD}-to-V_{SS} ESD clamp circuit and flows out of the IC from Dn2 to PAD2. See p. 2, lines 16-22. Cp1 and Cn1 reflect the parasitic junction capacitances of the diodes Dp1 and Dn1, respectively. See page 2, line 22 – page 3, line 6.

In contrast to the APA, the substrate-biased silicon diode (SBPD) in claims 8 and 23 provides higher ESD sustainability for ICs. The SBPD of the present invention is biased from the substrate for an improved turn-on speed of the SBPD and reduced leakage current. Unlike conventional diodes, an SBPD does not have a bottom junction capacitance and therefore exhibits a relatively smaller junction capacitance. In addition, because an SBPD is disposed over shallow trench isolations (STIs) in a silicon substrate, the silicon area used by the SBPD is reduced, which reduces cost. See p. 11, lines 5-11.

A well region 14 can be biased to control an SBPD 32 in accordance with embodiments of the present invention. See Fig. 4 and p. 12, lines 19-20. Likewise, a diffused region 20 can

also be biased to cause the well region 14 to be biased to control the SBPD 32. See p. 12, lines 21-22.

Fig. 11 shows an ESD protection circuit with two dual-SBPDs. For example, when an ESD current 4 is applied to Pad1, and with Pad2 grounded relative to Pad1, an ESD current 4 is conducted to VDD through silicon diode SBPD1. ESD current 4 is then discharged to the VSS line through a VDD-to-VSS ESD clamp circuit 6 and flows out of the IC through SBPD4. See p. 19, lines 3-12.

Fig. 12A show that the parasitic capacitance of the SBPD in accordance with the present invention is approximately half of the prior art polysilicon-bound diode (Fig. 1B), and Fig. 12B shows that the parasitic capacitance of the dual SBPDs (Fig. 11) is approximately half that of the dual polysilicon-bound diodes (Fig. 2). See page 20, lines 1-10. Accordingly, substrate biasing results in an improvement over the disclosed APA.

In order to anticipate a claim, the reference must teach each and every element of the claim, and "the identical invention must be shown in as complete detail as is contained in ... the claim." M.P.E.P. § 2131.

It is therefore, respectfully submitted, that independent claims 8 and 23 are not anticipated by the APA because the APA does not disclose or suggest each and every element of independent claims 8 and 23 – namely, the APA does not disclose substrate biased diode ESD protection for an IC. Claims 9-22 and 24-25 depend from claims 8 and 23, respectively. Accordingly, Applicant respectfully requests that the rejection of independent claims 1 and 23 and dependent claims 9-22 and 24-25 under 35 U.S.C. § 102(e) should be withdrawn.

Double Patenting

Claims 8-10 have been rejected under the judicially created doctrine of obviousness-type double patenting over claim 8 of U.S. Patent No. 6,690,065 ("the parent application").

Withdrawal of the rejection of claims 8-10 is respectfully requested for at least the following reasons.

The present application is a divisional application of U.S. Patent Application No. 09/749,377 which is now U.S. Patent No. 6,690,065 ("the parent patent"). Filed herewith is a Terminal Disclaimer in accordance with 37 C.F.R. § 1.321(b)-(c) setting forth the identity of the common assignee of the present application and the parent patent and disclaiming the terminal portion of any patent that issues in the present application beyond the expiration date of the parent patent.

The filing of the terminal disclaimer should not be construed to be an admission as to the validity of the substantive claim rejections cited above as the Applicants have presented substantive arguments that the claims of the present application are patentable over the APA.

Furthermore, the Examiner has acknowledged that claims 8-10 of the present application and claim 8 of the parent patent are not identical and that claims 8-10 are broader than claim 8 of the parent patent.

Accordingly, the rejection of claims 8-10 under the judicially created doctrine of obviousness-type double patenting has been overcome and should be withdrawn.

CONCLUSION

In view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including claims 8-10 and 15-25, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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April 19, 2006 By: Clark Jablon
(Date)

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